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Sequential Circuit Elements Using Reversible Logic Gates with MUX

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ABSTRACT: The reversible logic circuits are becoming popular in the design of low power digital circuits. The researchers building vital circuits required in advanced computing machines using reversible logic including DNA computing, optical information processing, quantum computation and nanotechnology. The sequential circuits are complex than combinational circuits since the output depends not only on present input but on the past input. It is proposed to replace basic gates with reconfigurable gate multiplexer to reduces delay. The proposed design of reconfigurable logic will improve h throughput area, power, and delay and garbage outputs. The modules has been coded with Verilog and simulated on ISE Design suite 14.7 and Modelsim.

KEYWORDS: Reversible logic gates, quantum computers, sequential circuits, latches, flip flops,mux.

I.INTRODUCTION

The Reversible logic is drawing attention due to its ability to reduce the power dissipation. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy [1]. Later Bennett, in 1973, claimed circuits built using reversible circuits can avoid kTln2 joules of energy dissipation in a circuit [2]. The integrated circuit would continue to improve unit cost by a factor of 2, every 18 months according to Gordon Moore[3], shrinking the dimensions on integrated structures increase the speed for the same power per unit area. The power dissipation in present day computing devices are becoming very high as more and more components are getting packed onto the chip.

The future technology would use reversible gates to reduce power[4]. Many people pursuing research in the area of reversible logic. Computers based mainly on reversible logic operations can reuse a fraction of the signal energy that theoretically can approach arbitrarily near to 100% as the quality of the hardware is improved[5].Like conventional digital circuits reversible logic circuits are classified into reversible combinational and reversible sequential circuits. Any arbitrary computational work and logic function can be realized using reversible in the same way it is done with conventional logic circuits. It is possible to build sequential computer with zero internal power dissipation using invertible logic gates[6].

A reversible logic circuit should be designed using minimum number of reversible logic gates and with minimum number of constant inputs [6-9]. Reversible logic gates can be used both in combinational and sequential circuits. In this paper we are presenting new reversible logic gates and the realization of reversible latches and reversible flip flops using these gates.

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II.BASIC DEFINITIONS PERTAINING TO REVERSIBLE LOGIC

Reversible logic gate:

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs [10]. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

Constant Input:

Constant inputs as name indicates the input are taken constant at 0 or 1. Constant input are the series of inputs, in reversible circuit constant input are used to make the number of inputs and outputs equal, so as to produce the stated logic function.

Garbage Output:

The additional numbers in outputs, inputs which can be added where ever necessary to compile the outputs is equal to inputs number. It can also be referred to as the output number which is not considerable in the synthesis of proposed function. It is a number which is additional in output so as to make n-input k-output reversible. We refer constant inputs to denote the value that are substituted (n: k) added to build function reversible. The method to show the relation between the constant input and garbage output is as shown below.

Input + k (Constant input) = Output + n (garbage output)

Delay:

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the assumptions that: (i) Each gate performs computation in one unit time and (ii) All inputs to the circuit are available before the computation begins.

Quantum cost:

Quantum cost is referred to the circuit cost in terms of cost of the primitive gate cost. Quantum cost can be calculated by understanding the number of primitive reversible logic gate (1 * 1 or 2 * 2) necessary to realize the circuits. Table 1 contains the list of Reversible gate, Size, Quantum cost of the gate and Functionality of the gate. Table 1 shows different type of reversible gate, size, quantum cost, and functionality [11].

Reversible Gates	Size	Quantum cost	Functionality
NOT	1X1	1	P=A'
CNOT(Feynman)	2X2	1	P=A Q=AxorB
Fredkin	3X3	5	P=A Q=A'B+AC R=AB+A'C
Toffoli	3X3	5	P=A Q=B R=ABxorC
Pears	3X3	4	P=A Q=AxorB R=AB xor C
Double Feynman	3X3	2	
NG	3X3	11	P=A Q=AB xor C R=A'C' xor B'

Table1: Parameter comparison of different Reversible gate

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III.PROPOSED WORK

The proposed work is realizing the basic gates with the multiplexer. When designing a reconfigurable gate multiplexer by replacing the basic gates we will get reduction in delay. The proposed design of the reconfigurable logic will improve the throughput of the circuit and also experiment result provides reduction in power and area in terms of LUTs.

Feynman gate

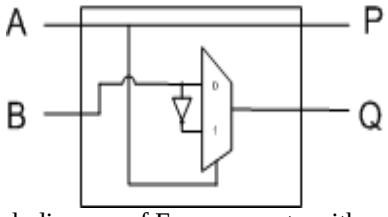

Figure 1: Block diagram of Feynman gate with mux realization
Output P=A,Q=A xor B

Fredkin Gate with multiplexer (mux) realization

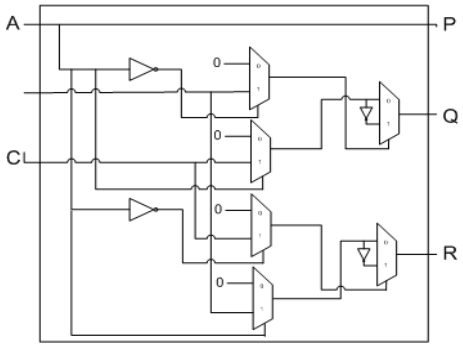

Figure 2:Block diagram of Fredkin gate using mux
Output P=A; Q=A'B+AC; R=AB+A'C

MS D Flip Flop Using Basic gates

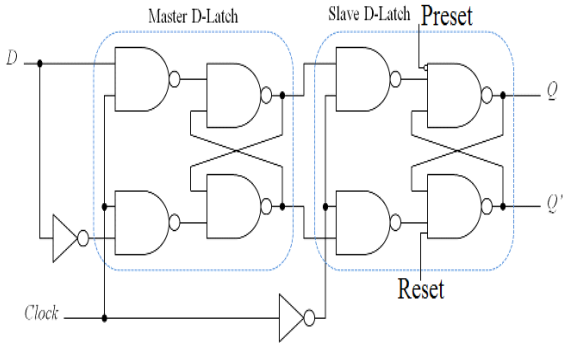

Figure 3: Block diagram of MS FF

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MS Flip Flop using reconfigurable gates

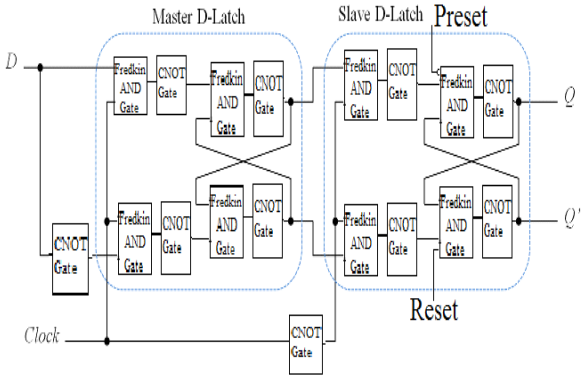

Figure 4:Block diagram of MS FF using reversible gate

Universal Shift Register 1

Universal shift registers store binary data either it may be zero or one, or when a clock signal is applied it can be shifted left or right. Depend upon the occurrence of the clock input All modes of operation such as serial-in serial-out (SISO), parallel-in parallel-out (PIPO) operation are performed. Figure5 shows the block diagram of universal shift register 1.Figure 5 shows the block diagram of Universal shift register[12].

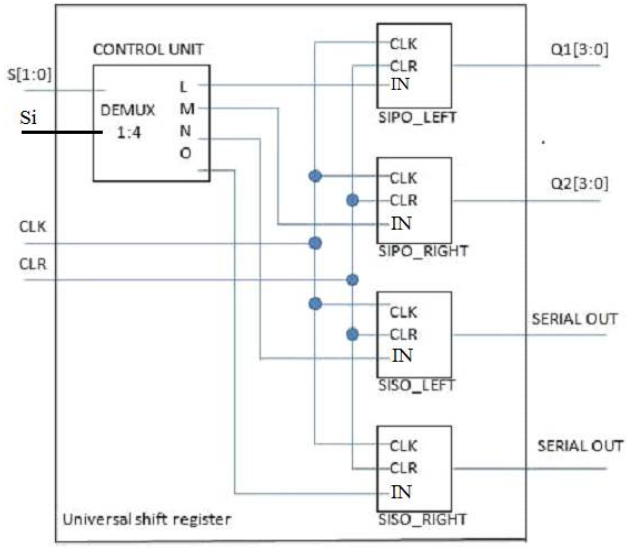

Figure 5:Block diagram of Universal shift register 1

our design consists of 4 D flip flop blocks, used to perform serial in parallel out left, serial in parallel out right, serial in serial out left and serial in serial out right respectively, and one 1 to 4 demultiplexer. The 1 to 4 demultiplexer have two common selection inputs S1 and S0. Depending upon the select line the respective operation performed when S[1:0] = 00 it perform SIPO-LEFT, S[1:0]=01 perform SIPO-RIGHT, S[1:0]=10 perform SISO-LEFT, S[1:0]=11 perform SISO-RIGHT. The present value of the register is applied to the D inputs of the flip flops. This condition forms a path from the output of each flip flop into the input of the same flip flop so that the output recalculates to the input in this form of operation.

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Universal Shift Register 2

The data in the universal shift register can be shifted left or right on the clock signal. The other modes of operation such as serial output left(SOL), serial output right (SOR), parallel output (PO) can also be performed depending upon the select line and occurrence of clock. Block diagram of Universal shift register shown in figure 6.

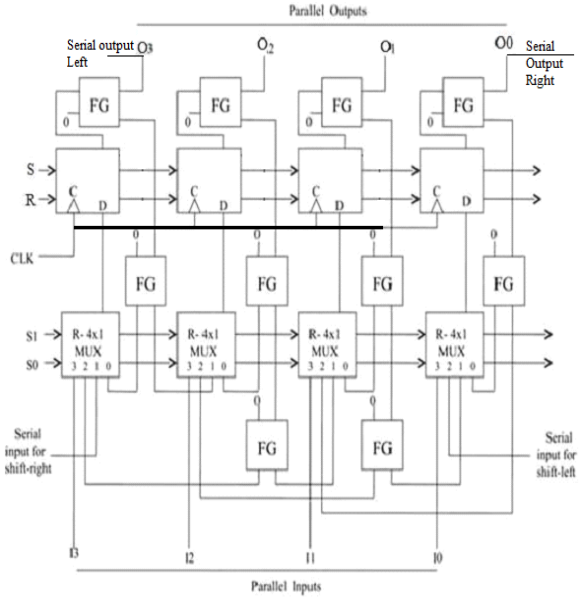

Figure 6:Block diagram universal shift register

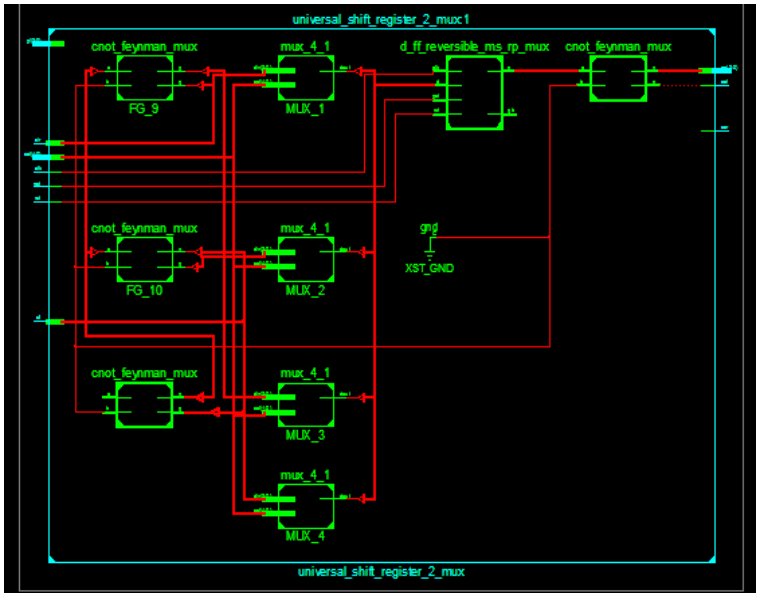

Figure7:Rtl schematic of universal shift register2_mux

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Serial Adder:

We have designed a universal shift register application serial adder shown in Figure 7. that adds two inputs serially and gives the serial output. It consists Serial In Serial Out (SISO) shift register. The block diagram of serial adder consists of two register, one full adder, and d-ff. For SISO shift register we have used the Universal Shift Register 2 with the selection lies to be S1 = 0 and S0 = 1 for making the universal shit register to behave as the SISO right shift register and the input is given to the serial in right. And the output is got from the serial output left. Serial adder is one which has delay less than that of parallel adder.

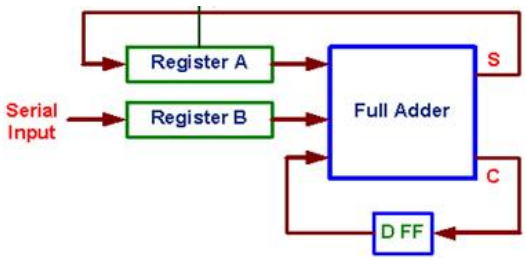

Figure 8:Block diagram of serial adder

IV.RESULTS

For the experiment considering the proposed Sequential Circuit Elements Using Reversible Logic Gates with MUX, the sequential circuit elements for serial adder using reversible gate with mux is designed using Verilog HDL and synthesized using Xilinx ISE 14.7.The experimental result shows optimal reduction performance of parameters such as Area in terms of LUTs and registers and delay in terms of nano seconds and power.

Parameter	Universal shift register reversible logic dff	Universal shift register reversible logic -mux
BELS	43	36
Delay	13.710ns	12.576ns
Power	14.68mw	14.59mw

Table 2:Result of universal shift register design 1

Parameter	Universal shift register reversible logic dff	Universal shift register reversible logic mux
BELS	16	12
Delay	16.154ns	15.660ns
Power	15.01mw	14.89mw

Table 3: Result of universal shift register design 2

Parameter	Serial Adder reversible logic mux
BELS	28
Delay	21.893ns
Power	14.30mW

Table 4: Result of serial adder

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V.CONCLUSION

The Research in the area of Reversible logic is on the prior due to the capability of the reversible logic to lessen the power dissipated which has resulted in loss less circuits. Our proposed sequential circuit element using reversible logic gate with mux realization .the experimental result shows successful reduction in area, delay and power.

VI.FUTURE SCOPE

Sequential circuit element using reversible logic gate with mux realization can be design with using different reversible logic gateand using mux realization and get the improved results, also the proposed design can also be extended to a 8-bit Reversible Universal shift Register.

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